AN4399

Advice on using the SL6619

Application Note

AN4399 - 1.6 April 1996

INTRODUCTION

This application note outlines a basic circuit for the SL6619 Direct Conversion Pager Receiver for use in standard paging applications at 153MHz, 282MHz and 450MHz. An Evaluation Board based on 282MHz will be described and detailed set-up procedure provided.

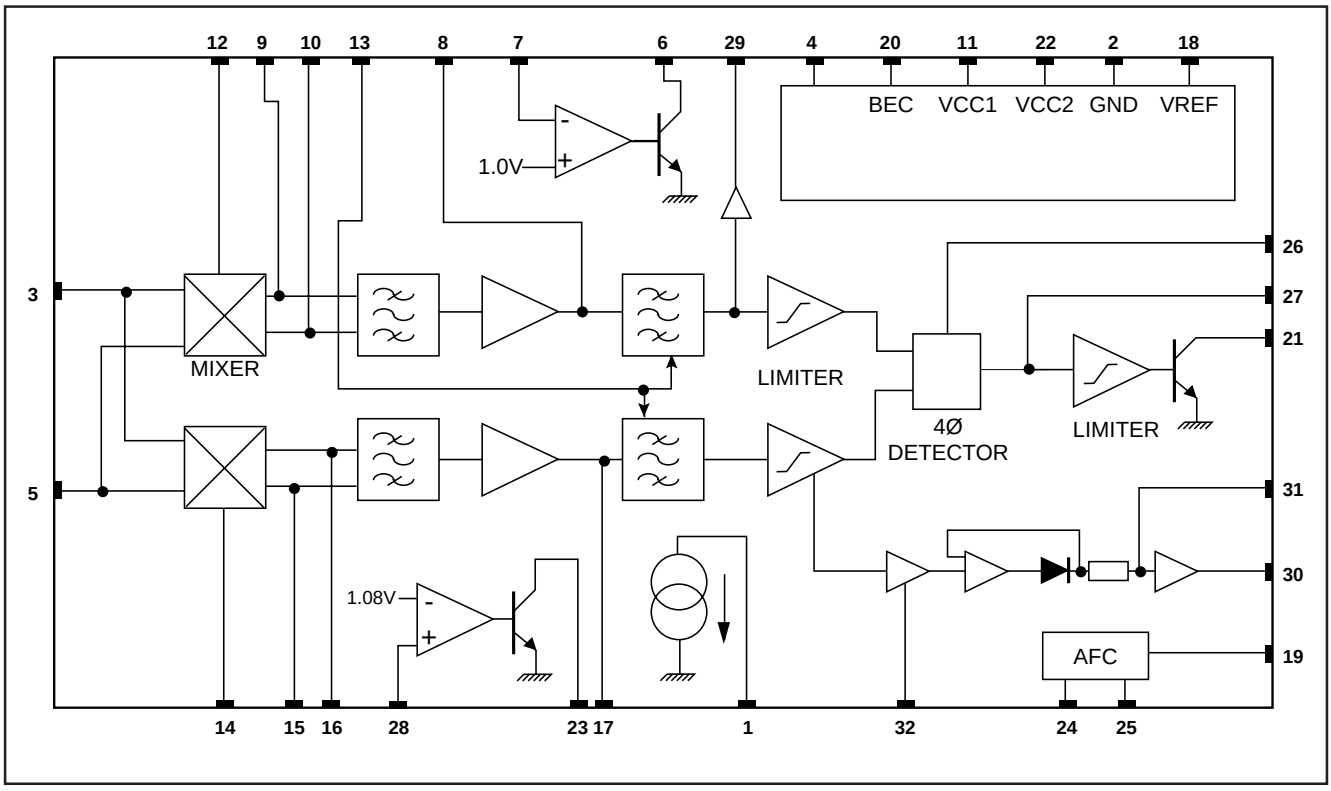


Fig.1 block diagram

PIN DESCRIPTION

Pin No	Pin Name	Pin Description	Pin Details
1	IRF	RF Current Source	An on-chip current source for use in RF amplifier designs. This allows the current in the RF amplifier to be independent of supply voltages. The current source incorporates an RF signal AGC. This ensures optimum operation of the device for high input signal levels. See “Circuit Facilities”.
2	GND	Receiver Ground	Ground for receiver RF circuits
3	MIXIP A	Mixer Input A	Input to the device from an external RF amplifier. The signal should be applied differentially between Pin 3 and Pin 5. The differential signal to the mixers may be DC coupled if no DC voltage is applied, otherwise AC coupling should be used.
4	MIX DEC	Mixer Bias Decouple	External decoupling for the mixer bias.
5	MIXIP B	Mixer RF Input B	Differential input from an external RF amplifier. See Pin 3.
6	REG CNT	Voltage Regulator	1V on-chip regulator output. Used to Control OP drive a suitable PNP transistor. See “Circuit Facilities”. For stability purposes a capacitor should be applied between Pin 6 and Pin 7. The regulator is only specified for Vcc1>=1.1V.
7	VREG	Voltage Regulator Sense	This should be connected to the load of the regulator. If the regulator is not required, and no active components are connected to Pin 6 and Pin 7, then Pin 7 should be connected to Vcc2.
8	TPI	Channel I Test Point	Channel I internal amplifier Pre-Gyrator output/Gyrator filter input. This pin is used to measure the receiver signal level during receiver set-up. It may also be used in conjunction with Pin 29 (TPLIMI) to measure the response of the Gyrator filters. It can be used, if necessary, to add additional filtering in the channel in the form of an additional external capacitor.
9	I1	Mixer Output 1, I Channel	One of the two I channel differential outputs. Additional filtering between the outputs can be added by having an external capacitor between Pin 9 and Pin 10 (See Application Circuit Requirements).
10	I2	Mixer Output 2, I Channel	See Pin 9
11	VCC1	Supply 1 Connection	Vcc1 supply. This requires adequate Audio and RF decoupling if optimum device sensitivity is to be achieved.

12	LOIP I	LO Input Channel I	The local oscillator signal is applied to Pin 12 in phase quadrature to Pin 14. For the phase quadrature circuit see “Application Circuit Requirements”. The LO input of the mixer requires a bias path to Vcc1.
13	GYRI	Gyrator Filter Adjust	The bandwidth of the on-chip gyrator filter can be adjusted using a resistor from Pin 13 to GND. For values of resistor against gyrator bandwidth see “ Circuit Facilities”.
14	LOIP Q	LO Input Channel Q	See Pin 12
15	Q1	Mixer Output 1, Q Channel	One of the two Q channel differential outputs. Additional filtering between the outputs can be added by having an external capacitor between Pin 15 and Pin 16 (See Applications Circuit Requirements).
16	Q2	Mixer Output 2, Q Channel	See Pin 15
17	TPQ	Channel Q Test Point	Channel Q internal amplifier Pre-Gyrator output/Gyrator filter input. This pin is used to measure the receiver signal level during receiver set-up. It can be used, if necessary, to add additional filtering in the channel in the form of an additional external capacitor.
18	VREF	Reference Voltage	This voltage reference (1.25V) may be used to bias external RF amplifier. See “Circuit Facilities” for details.
19	AFC OP	AFC Output	This is a charge pumped current output, the DC component of which, after integration gives the AFC control signal to drive a varactor. See “Circuit Facilities” for details
20	BEC	Battery Economy Control	The battery economy facility allows the device to be powered down by pulling Pin 20 to GND. If not required this should be connected Vcc2
21	DATA OP	Data Output	Open collector data output. This requires a pull-up resistor to a suitable voltage reference e.g. Vcc2.
22	VCC2	Supply 2 Connection	Vcc2 supply to the receiver. This pin requires adequate audio decoupling to GND. If a DC-DC converter is used to generate this voltage care must be taken to prevent power supply noise reducing the sensitivity of the device.
23	BATT FLAG	Battery Flag Output	The battery flag is the output of an on-chip comparator with VREF as the reference voltage. When VBATT (Pin 28) > VREF, Battery Flag Output is Low. BATT FLAG is an open collector output. This requires a pull-up resistor to a suitable voltage reference e.g. VCC2.

24	AFC1	AFC Characteristic Defining Pin 1	The combination of resistor/capacitor on Pin 24 and Pin 25 define the sense and shape of AFCOP characteristic. See " Circuit Facilities" for details.
25	AFC2	AFC Characteristic Defining Pin 2	See Pin 24
26	BRF CNT	Bit Rate Filter Control	A tri-state input to enable 3 baud rates to be implemented with any component change.
27	BRF1	Bit Rate Filter Output from Detector	Output of the phase detector. For optimum performance a Bit Rate Filter can be applied to this pin. This is achieved by applying a capacitor between Pin 27 and VCC1. See "Circuit Facilities" for the value of the capacitor and the corresponding setting on Pin 26.
28	VBATT	Battery Flag Input Voltage	Connect this pin to Pin 11 (VCC1) if a 1.08 volt threshold is required. Alternative thresholds may be determined using an external potential divider. See "Circuit Facilities" for details
29	TPLIMI	I Channel Post Gyrator Filter Test Point, Output Only	This pin provides a monitor of the gyrator filter output of channel I, to enable the response of the filter to be accurately measured and adjusted using Pin 13. For details refer to "Setting Up Procedure".
30	IAGC OP	Audio AGC Output Current	A current source controlled by the Audio signal level and the AGC threshold adjust (Pin 32). The current source is intended to sink current from an PIN diode on the RF input and hence reduce the RF signal incident on the RF amplifier input to preserve IM performance at high RF level.
31	TC ADJ	Audio AGC Time Constant Adjust	The attack (turn on) and decay (duration) times of the Audio AGC are set by an RC network connected to Pin 31. See "Circuit Facilities" for details.
32	GTH ADJ	Audio AGC Gain and Threshold Adjust (RSSI Signal Indicator)	Level adjustment for the external AGC drive. See "Circuit Facilities" for details.

CIRCUIT FACILITIES

RF Current Source - IRF

With the pin connected to a potential of 0.2V (i.e. the emitter of a transistor with the base voltage Vb = 1V (e.g. VREG)), the current is nominally set to give IRF = 500µA.

The RF current source incorporates an RF signal AGC which is an automatic gain control loop that protects the mixer's RF inputs, Pin 3 and Pin 5, from large out of band RF signals.

The loop consists of an RF received signal strength indicator which detects on the signal at the inputs of the mixers. This RSSI signal is then used to control the RF current source. At an RF level around 25mVrms at the mixer inputs (Pin 3 and Pin 5) the current source begins to reduce its current output.

Voltage Regulator Control - REG CNT

The on-chip regulator should be used in conjunction with a suitable PNP transistor to achieve regulation. As the transistor forms part of the regulator feedback loop the transistor should exhibit the following characteristics:-

$$H_{FE} > 100 \text{ for } V_{CE} >= 0.1V$$

If no external PNP transistor is used, the maximum current sourcing capability of the regulator is limited to 20µA.

Reference Voltage - VREF

This on-chip voltage reference VREF (1.2V) may be used to bias an external RF amplifier and as a reference for IRF (Pin 1) to form an RF AGC circuit. VREF can source a maximum current of 20µA but should not be used to sink current.

Gyrator Filter Adjust - GYRI

The on-chip filters include an adjustable gyrator filter. This may be adjusted with the use of an additional resistor between Pin 13 and GND. This allows flexibility of filter characteristics and also allows for compensation for possible process variations. The overall 3dB bandwidth of the gyrator filter is proportional to 1 / R (R = resistor value between Pin 13 and GND). Typical values of R against F_{3dB} for normal applications are:-

R(Ohm)	F_{3dB}(kHz)
120K	11.5
150K	9.7
180K	8.1
220K	6.6

Audio AGC - IAGC_OP, TCADJ & GTHADJ

The internal structure associated with the Audio AGC facility is shown in Fig.2.

The Audio AGC facility consists of a current sink which is controlled by the audio (baseband) signal amplitude. It has three parameters that may be controlled by the user; the Attack (turn on) time, Decay (duration) time and threshold level.

The Attack time is simply determined by the value of the external capacitor connected to Pin 31 (TCADJ). The external capacitor is in series with an internal 100k Ohm resistor and the time constant of this circuit dictates the attack time of the AGC.

$$\text{i.e. } T_{ATTACK} = 100k * C_{TC}$$

The Decay time is determined by the external resistor RDECAY connected in parallel to the capacitor CTC. The Decay time is simply T DECAY = RDECAY * CTC

When a large audio (baseband) signal is incident on the input to the AGC circuit (Fig.2) the variable current source is turned on. This causes a voltage drop across R9. The voltage potential between VREF and the voltage on Pin 32 causes a current to flow from Pin 31. This charges up CTC through the 100k internal resistor. As the voltage across the capacitor increases, current source 2 is turned on and this sinks current from Pin 30.

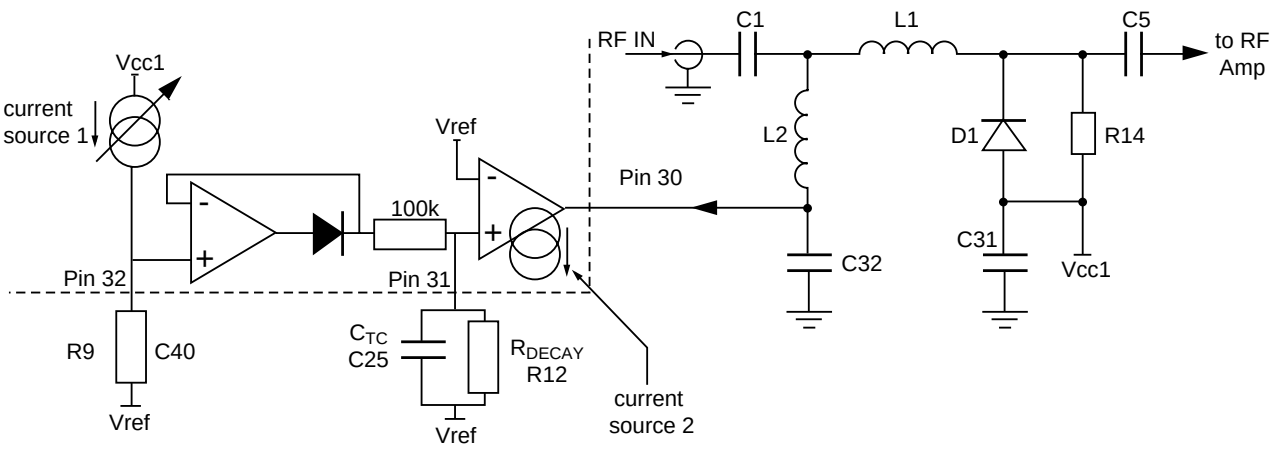
The current sink on Pin 30 can be used to drive the external AGC circuit by causing a PIN diode to conduct, reducing the signal to the RF amplifier.

The relationship between the incident audio signal and current source 1 is shown in Fig.3. This can be used in conjunction with the value of R9 to set the voltage at Pin 32 for any particular signal level.

The relationship between the voltage at Pin 32 and the output of current source 2 is given in Fig.4.

Using both figures, the value of R9 can be selected to give the required output current at Pin 30 for any particular input signal level. Note, however, that the maximum Audio signal and hence the Audio AGC current (Pin 30) is limited in practice by a typical receiver gain distribution to approximately 45µA.

The Audio AGC may be simply disabled by connecting Pin 32 (GTHADJ) to VREF. Alternatively by connecting Pin 30 (IAGCOUT) to Vcc2 and connecting Pin 31 (TCADJ) directly to VREF. This would then allow the use of the voltage drop across 9, when connected to Pin 32, to be used as an RSSI (Receiver Signal Strength Indicator (Audio)). Fig.5 shows typical response of the Audio AGC with wanted and unwanted signal level.



AGC Components Values (282MHz)

R9	=	33K	C1, C5, C31, C32	=	1n
R12	=	220K	C25		See Note
R14	=	47K	C40	=	100n
			L1	=	33nH
			L2	=	820nH
			D1	=	MA862 (Panasonic) or DAP236K (Rohm)

Note: R9 sets the gain (sensitivity) of the Audio AGC. If R9 is increased then the Audio AGC will become active for a lower wanted signal level. Increasing R9 can cause the Audio AGC loop to become unstable. C25 should then be increased to increase the turn on/off time to prevent oscillation occuring.

Fig.2 Audio AGC Schematic

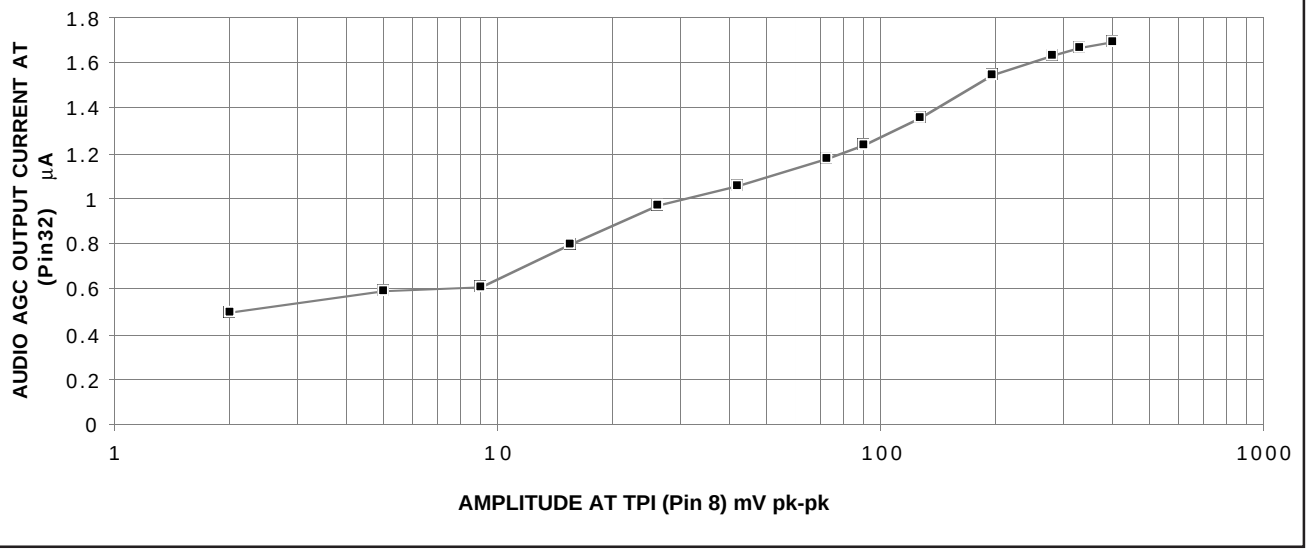


Fig.3 RSSI Audio AGC vs TPI (Pin 8)

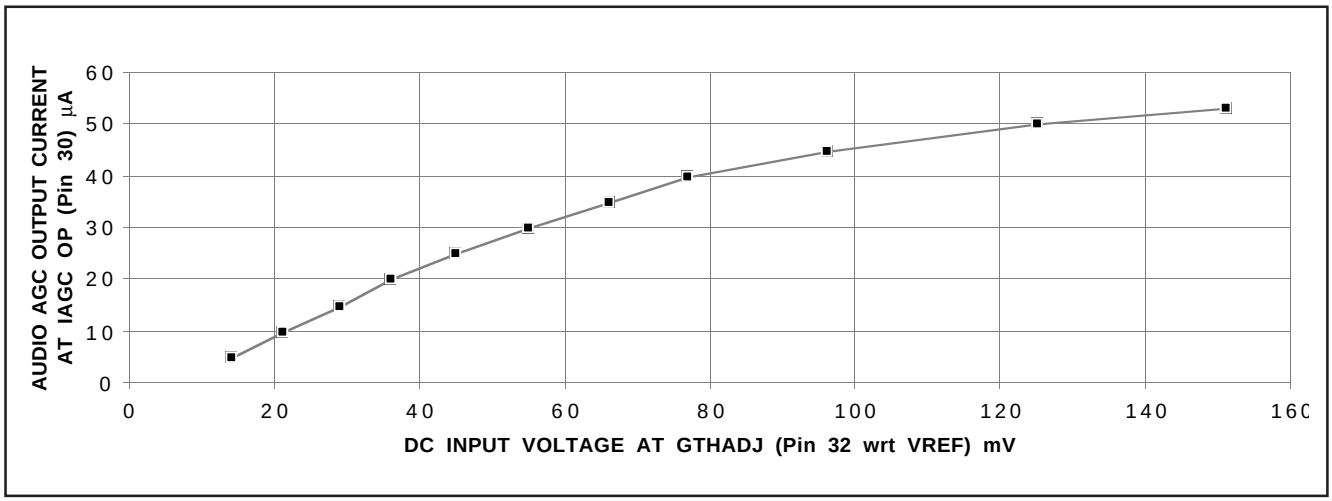


Fig.4 Audio AGC Current IAGC OP vs DC Voltage at GTHADJ

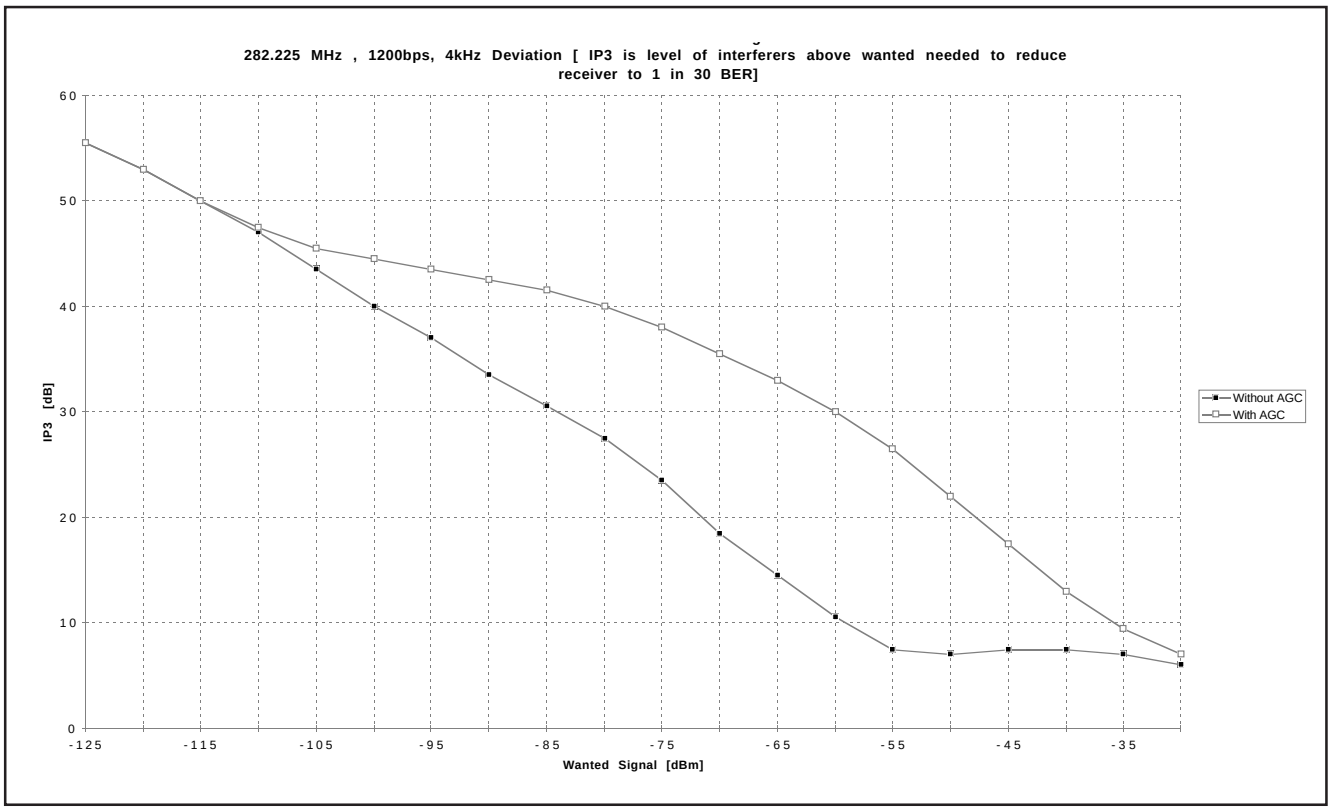


Fig.5 SL6619 IP3 vs Wanted Signal

Battery Flag Input - VBATT

The battery flag threshold may be simply increased by using a suitable potential divider so that at the required battery threshold voltage, the voltage at Pin 28 (VBATT) is 1.08V.

Bit Rate Filter Control - BRF CNT & BRF1

The logic level on Pin 26 controls the cut off frequency of the 1st order bit rate for a given bit rate filter capacitor at Pin27. This allows the cut-off frequency to be changed between Fc, 2 X Fc and 0.43 X Fc through the logic level on Pin 26.

This function is achieved by changing the value of the current in the 4-phase detector's output stage. A logic zero (0V to 0.1V) on Pin 26 gives a cut-off frequency of Fc, a logic one (Vcc2-0.3V to Vcc2) gives a cut-off frequency of 2 X Fc and an open circuit connection to Pin 26 gives a cut off frequency of 0.43 X Fc.

For example:-

Bit Rate Filter capacitor at Pin 27 =	560pF
Level on Pin 26	Baud Rate
Logic Zero (0V)	512 bps
Open Circuit	1200 bps
Logic One (Vcc2)	2400 bps

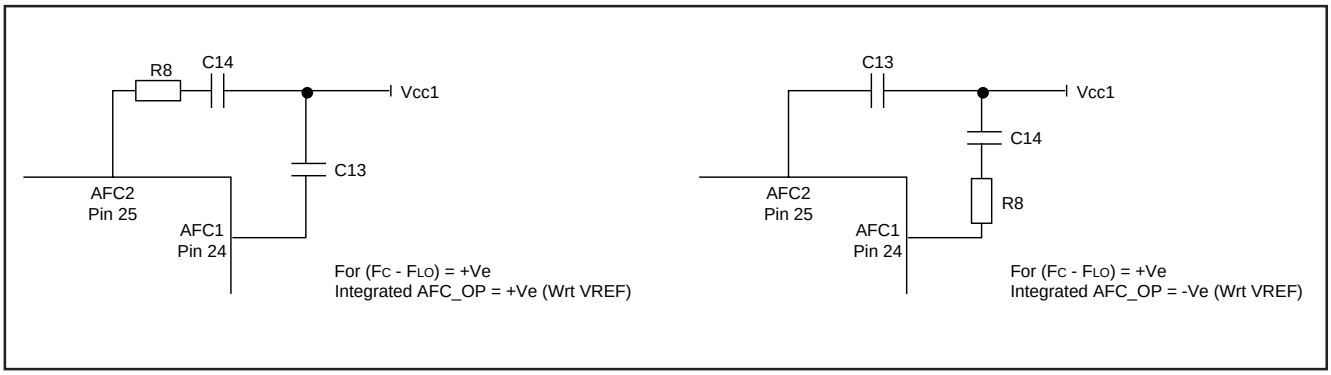


Fig.6 AFC1 & AFC2 Characteristics

Automatic Frequency Control - AFC1, AFC2 & AFC OP

The on-chip AFC circuit is a negative feedback loop which requires an external integrator (capacitor) to complete the control function.

The resistor / capacitor networks on AFC1 (Pin24) and AFC2 (Pin 25) define the open loop characteristic.

The AFC circuit tries to maintain the IF frequency equal to a frequency that is defined by components C13, C14 and R8 (Fig.6) at all time. The frequency defined by these components is set to the peak deviation of the FSK modulated input signal.

In a Direct Conversion Receiver demodulating an FSK signal, the instantaneous IF frequency is equal to $\Delta F + (F_C - F_{LO})$ or $\Delta F - (F_C - F_{LO})$ depending on whether the incoming signal is a logic 1 or 0. The feedback loop adjusts the LO frequency such that the IF frequency is equal to ΔF, which implies $F_C - F_{LO} = 0$.

Fig.7 shows the open loop characteristic measured with preamble (010101 data stream) at 1200 bps. The shape of this characteristic is defined by the resistor / capacitor networks on AFC1 and AFC2. The recommended components are as follows:-

4 kHz	Peak Deviation:	
	560pF	on AFC1
	15kOhm in series with 1.5nF	on AFC2
4.5 kHz	Peak Deviation:	
	470pF (490pF)	on AFC1
	15kOhm in series with 1.2nF (1.33nF)	on AFC2

The polarity of the open loop characteristic can be reversed by swapping over the components on AFC1 and AFC2 or alternatively by swapping over the phase of the LO signals LOI relative to LOQ.

The AFC_OP is a charge pumped current output, after this is integrated by an external capacitor C29 (between AFC_OP and VREF) a DC voltage is produced. This voltage is then used to control an VCXO via a varactor, for example.

The AFC_OP must be buffered if it is to drive a signal generator via an external modulation input for experimental purposes. Any significant loading on AFC_OP pin will distort the AFC's open loop characteristic.

Within the feedback loop there are conditions where polarity change can occur resulting in positive feedback rather than negative feedback. This will make the difference between F_C and F_{LO} larger rather than nulling it. In general this condition only arises if the initial frequency offset (F_C-F_{LO}) is greater than ΔF or in the presence of large interfering signals. If the AFC loop fails to capture it is most likely due to positive feedback. Fig.7 shows the positive feedback area where (F_C-F_{LO}) > ΔF. When the receiver is cycled using the BEC facility the AFC_OP resets to a known voltage level of VREF (1.25V) upon startup. Then the AFC loop becomes active and produces the necessary control voltage for the VCO.

APPLICATION CIRCUIT REQUIREMENTS

The example application circuit is shown in Fig.8. To achieve optimum performance of the device it is necessary to incorporate a Low Noise RF Amplifier at the front end of the receiver. This can be biased using the on-chip voltages and current source provided.

RF Amplifier

The design of the RF amplifier is simplified by the on-chip current source and the two voltage references VREF and VREG.

A suitable circuit in cascode configuration is shown in Fig.9. The current through the load and hence the gain of the amplifier is controlled by the on-chip current source IRF. This ensures that the gain of the amplifier is independent of the supply voltage. Also, as VREF and VREG are independent of supply voltage it ensures that the bias points of the transistors are also stable and independent of supply voltage, with each transistor simply biased via a series resistor to the appropriate voltage reference.

The RF amplifier current source (Pin 1) forms part of the RF AGC circuitry reducing the RF amplifier current if excessive signal is incident on the mixer inputs. It is important to use the current source in the design of the RF amplifier. This ensures that the SL6619 will operate with high level input signals.

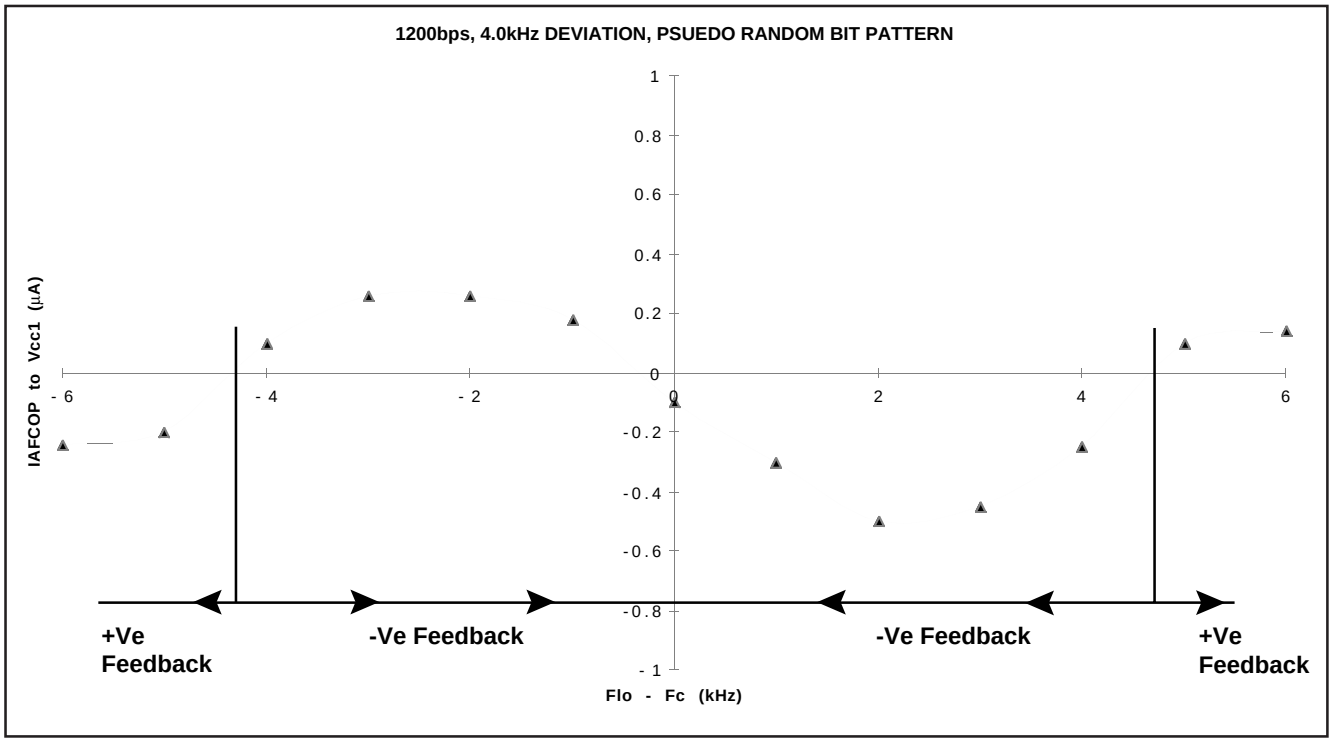


Fig.7 AFC Open-loop characteristic

The differential input required by the mixers is applied from the RF amplifier via a suitable transformer (T1). This forms a tuned load with the variable capacitor (VC1). This load is tuned to the operating frequency of the device. The maximum overall gain of the amplifier is also controlled by the load resistor (R13) in parallel with the transformer.

An LC coupling network can be used to replace the transformer (T1) in the application circuit. This couples the RF amplifier output to the mixer inputs (Pin 3 and Pin 5). The circuit is shown in Fig.10.

Local Oscillator Network

The local oscillator signal is applied to the device in phase quadrature. This can be achieved with the use of two RC network operating at their -3dB / 45 degrees transfer characteristic at the local oscillator frequency, giving a full 90 degrees phase differential between the LO ports of the device (see Fig.11). Each LO port of the device also requires an equal level of drive from the oscillator. In this applications circuit the local oscillator is applied by a signal generator with a source impedance of 50 Ohm hence the total RC network (including mixer bias) is designed to have this input impedance.

RF and Audio Decoupling Requirements

All voltage and current sources used for bias of the RF amplifier and receiver mixers should be decoupled at RF and Audio (baseband) frequencies using suitable capacitors. RF decoupling should be as close as possible to the RF circuit.

Open Collector Outputs

The Data Output and the Battery Flag output are open collector and require a pull-up resistor to a suitable voltage reference. Care must be taken to ensure that the pull-up resistor is adequate to supply sufficient current to the load. Also the routing of the Data Output line should be kept to a minimum to avoid radiation of the transition spikes.

Additional Adjacent Channel Rejections

There is an internal resistor between Pin 10 & 9 and Pin 16 &15, which when combined with an external capcitor can provide additional filtering to improve adjacent channel rejection performance. The capacitor value of 4.7nF used in the application circuit provides a 3dB cut-off point at about 19kHz.

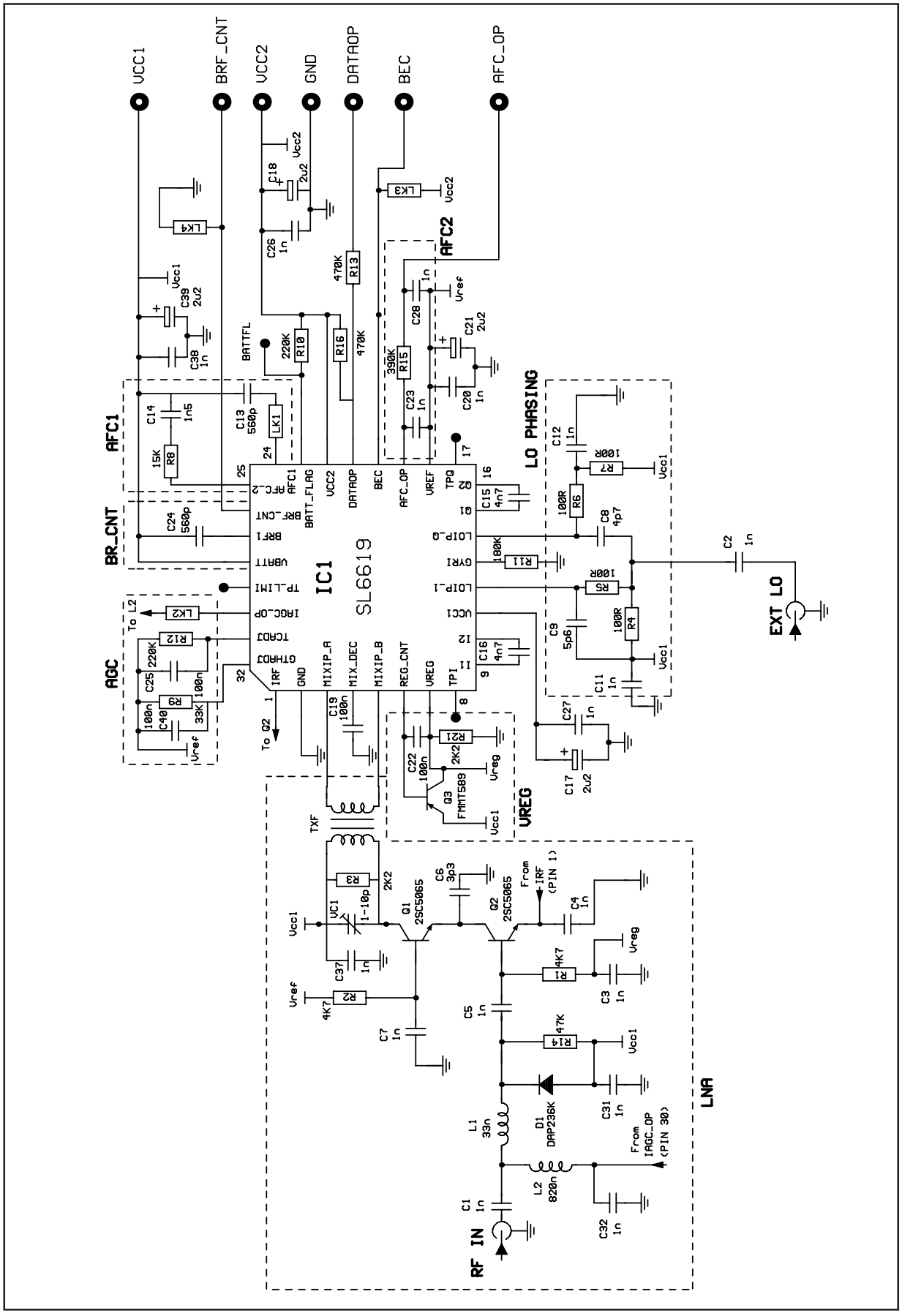
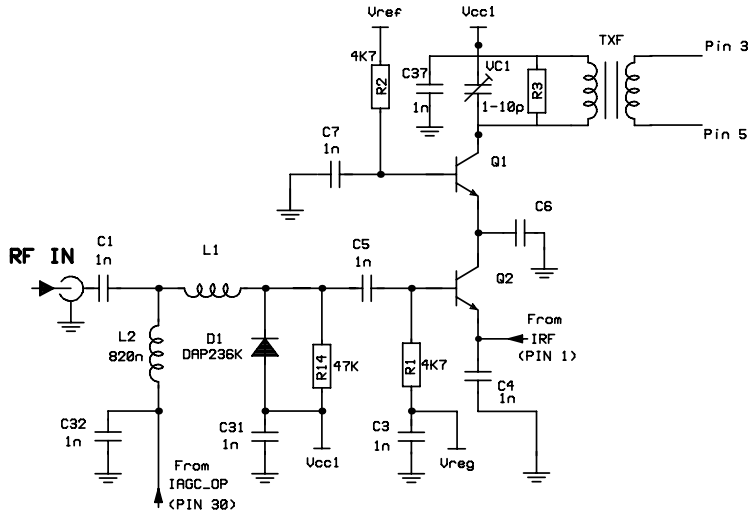


Fig.8 Basic Applications Circuit for 282MHz using External LO

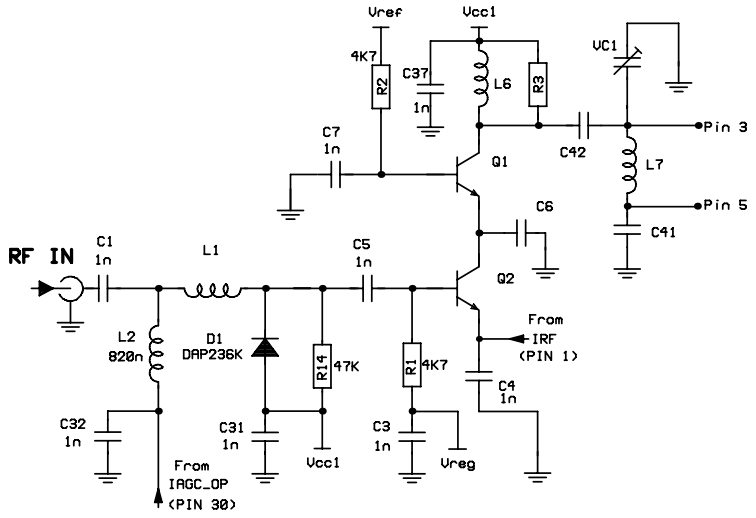


Frequency Dependent Components

	153MHz	282MHz	450MHz
L1	100nH	33nH	47nH
C6	3p3	3p3	1p8
TXF	100nH	30nH	16nH
	CoilCraft N2261-A	CoilCraft M1686-A	CoilCraft Q4123-A
Q1, Q2	Toshiba 2SC5065	Toshiba 2SC5065	Philips BFT25A

Note: The value of R3 is set such that when the RF input signal is at -73dBm with an off-set of 4kHz, the level at the test point (TPI or TPQ) should be 290mV ± 10mV.

Fig.9 RF Amplifier

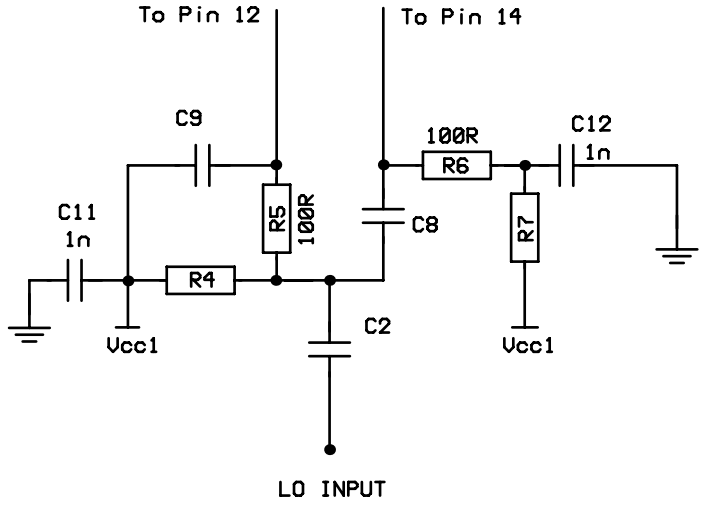


Frequency Dependent Components

	153MHz	282MHz	450MHz
L1	100nH	33nH	47nH
L6	150nH	82nH	47nH
L7	330nH	100nH	39nH
VC1	1-10pF	1-10pF	not used
C42	1nF	1nF	1-5pF
C41	2p7	3p3	10p
Q1, Q2	Toshiba 2SC5065	Toshiba 2SC5065	Philips BFT25A

Note: The value of R3 is set such that when the RF input signal is at -73dBm with an off-set of 4kHz, the level at the test point (TPI or TPQ) should be 300mV ± 10mV.

Fig.10 RF amplifier with mixer transformerless matching circuit



Frequency Dependent Components

	153MHz	282MHz	450MHz
C8	10p	5p6	3p3
C9	10p	5p6	3p9

For External LO Injection (50Ω input impedance)
C2 = 1n
R4, R7 = 100R

For Crystal Oscillator Input (higher input impedance)
C2 is set by load allowable on crystal oscillator (typical 4p7)
R4, R7 = 100R

Fig.11 Local Oscillator Network

EVALUATION BOARD SETTING UP PROCEDURE

INTRODUCTION

The Evaluation Board has been designed so that when fully populated all major functions of the SL6619 can be evaluated.

A set of procedures is described with which a number of measurements can be made on the Evaluation Board. The result of the measurements can then be compared with those provided by Mitel.

There are 3 different evaluation board options:

Option	Functions included	Functions NOT included
1	AGC Circuitry/RSSI AFC Circuitry AFC Buffer	AGC PIN diode LO / VCXO
2	AGC Circuitry including PIN diode AFC Circuitry AFC Buffer	LO / VCXO
3	AGC Circuitry including PIN diode AFC Circuitry AFC Buffer LO / VCXO	

The schematic of the Evaluation Board is shown in Fig. 12 which is divided into 8 functional blocks for easy reference. A brief description of each block is given below.

LNA
LO PHASING
VREG
AGC
AFC1
AFC2
AFC BUFFER
LO / VCXO
BR_CNT

LNA

The Low Noise Amplifier consists of two RF NPN transistors in cascode configuration. VC1 tunes for maximum output to the mixers and R3 sets the maximum overall gain of the amplifier. The LNA on the Evaluation Board uses the on-chip current source Pin 1 which is set to provide a current of 500uA. At high RF input level (well above sensitivity) the current source reduces the LNA gain by decreasing the supplied current. This in turn reduces the RF input to the mixers and hence limits the amount of current drawn by the mixers.

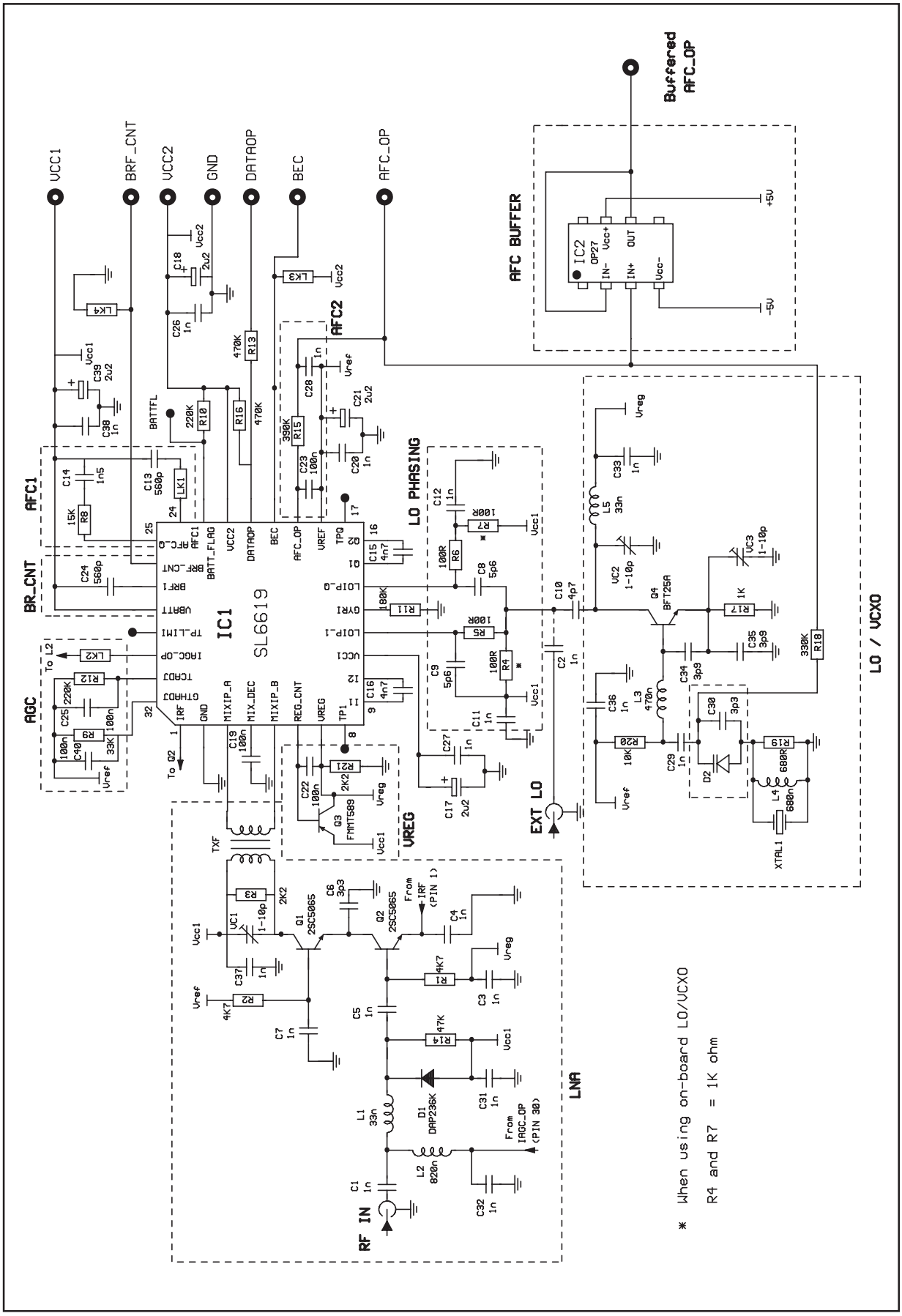


Fig.12 Evaluation Board Schematic

LO Phasing

The Local Oscillator signal is applied to the device in phase quadrature. This can be achieved with the use of two RC networks operating at their -3dB/45degrees transfer characteristic. The RC characteristics for I and Q channels are combined to give a full 90 degrees phase differential between the LO port of the device. Each LO port of the device also requires an equal level of drive from the oscillator. This is achieved by forming the two RC networks into a power divider. The board is set up to use an external local oscillator hence the EXT LO port is set at 50 Ohm.

VREG

The on-chip regulator is used in conjunction with the FMMT589 PNP transistor (HFE >100 for VCE>=0.1V) to provide a 1V regulated supply for the LNA and the LO / VCXO. If no external PNP transistor is used, the maximum current sourcing capability of the regulator is limited to 20uA. If the LO / VCXO is not present to taking a minimum current from the regulator a 2K2ohm dummy load (R21) is required to prevent oscillation.

Audio AGC

The Audio AGC consists of a current sink which is controlled by the audio (baseband) signal. It has three parameters that may be controlled by the user. These are the Attack (turn on) time, Decay (duration) time and Threshold level. Details on these parameters can be found in the Data Sheet.

The AGC control current provided at PIN 30 is used to drive the PIN diode D1. Due to the limited current available from Pin 32 the PIN diode used is in fact a band-switching diode which can be turned on at relatively low current level. The input RF level at which the diode cuts in will depend upon the type of diode and the value of R14. See Fig.2

AFC1

This part of the AFC circuit controls the Open Loop characteristic i.e. AFC_OP current vs (F_{LO}-F_C).

For peak deviation frequency of 4 KHz, the recommended component values are:-

Pin24 - AFC_I 560pF
Pin25 - AFC_Q 15K in series with 1.5nF

For peak deviation frequency of 4.5 KHz, the recommended component values are:-

Pin24 - AFC_I 470pF(490pF)
Pin25 - AFC_Q 15K in series with 1.2nF(1.33nF)

The polarity of the open loop characteristic can be reversed by swapping over the components on 'AFC_I' and 'AFC_Q' or alternatively by swapping over the phase of the LO signal LOI relative to LOQ. The components in the AFC1 sub-circuit on the Evaluation Board is arranged such that the current output is positive for Fc higher than Flo. Spaces are provided on the board so that it is possible to change the polarity if required. Fig.13 shows a typical closed-loop control voltage characteristic using an external DCFM signal generator.

AFC2

The AFC_OP is effectively a charge pump output. The polarity of which, as mentioned above, depends upon the AFC1 circuitry and the sense of (F_C - F_{LO}). The frequency of the charge pump is related to the magnitude of (F_C- F_{LO}). An integrator is required to turn the current pulses from the AFC_OP into voltage for VCO control purposes. This is done by the sub-circuit AFC2. The time constant of this circuit combined with that of the VCXO sets the overall time constant of the AFC under closed loop condition. Fig.14 shows a typical sensitivity vs frequency offset characteristic with and without AFC. Fig.15 shows the probablitiy of capture of a closed-loop AFC under BEC cycling condition.

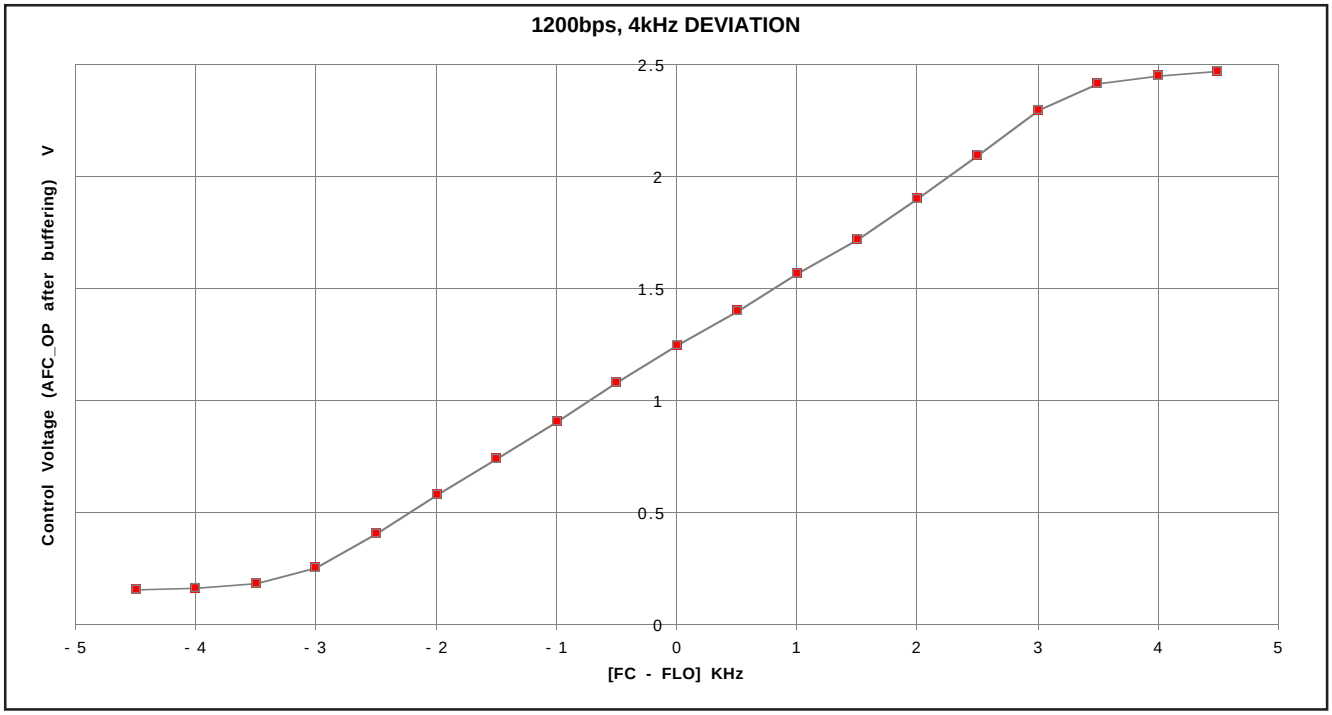


Fig.13 Typical AFC closed-loop control voltage characteristic

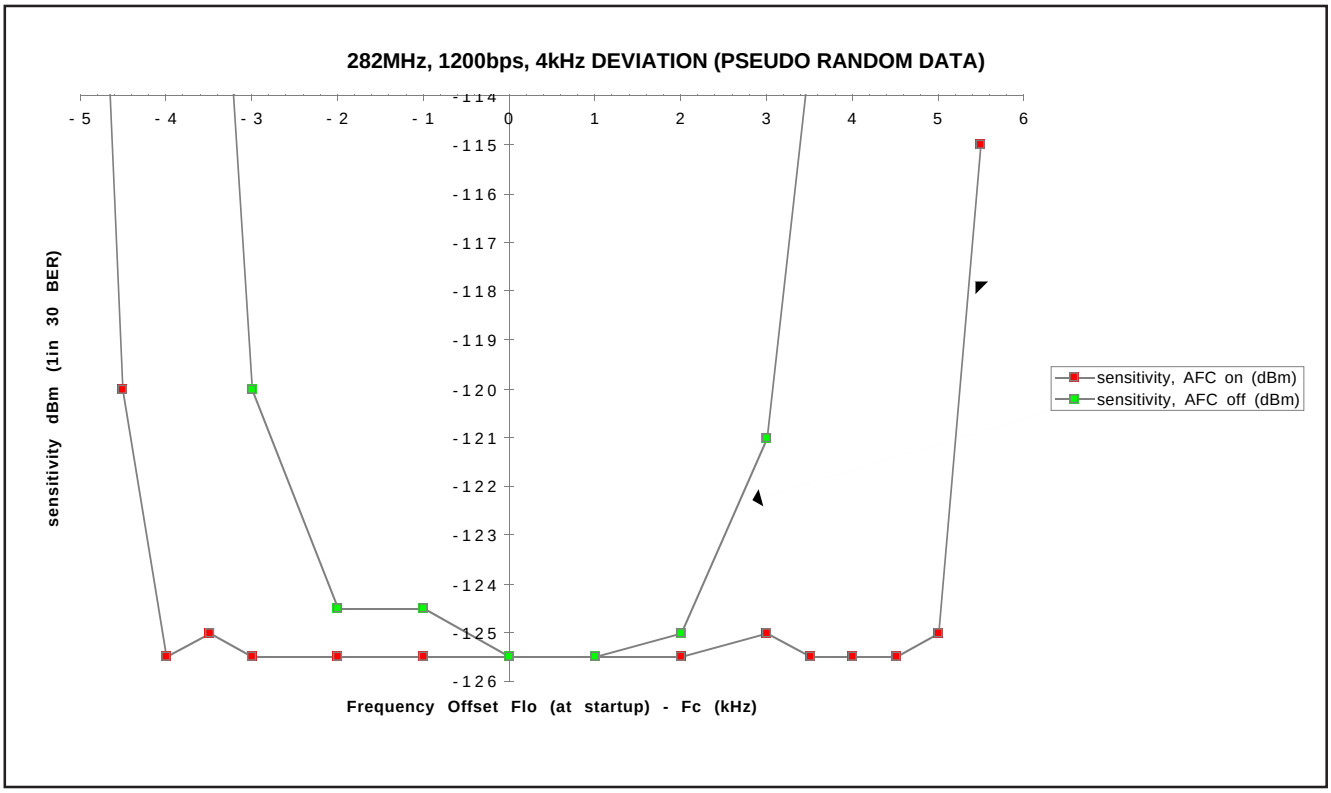


Fig.14 Typical Sensitivity vs Frequency offset with AFC ON/OFF

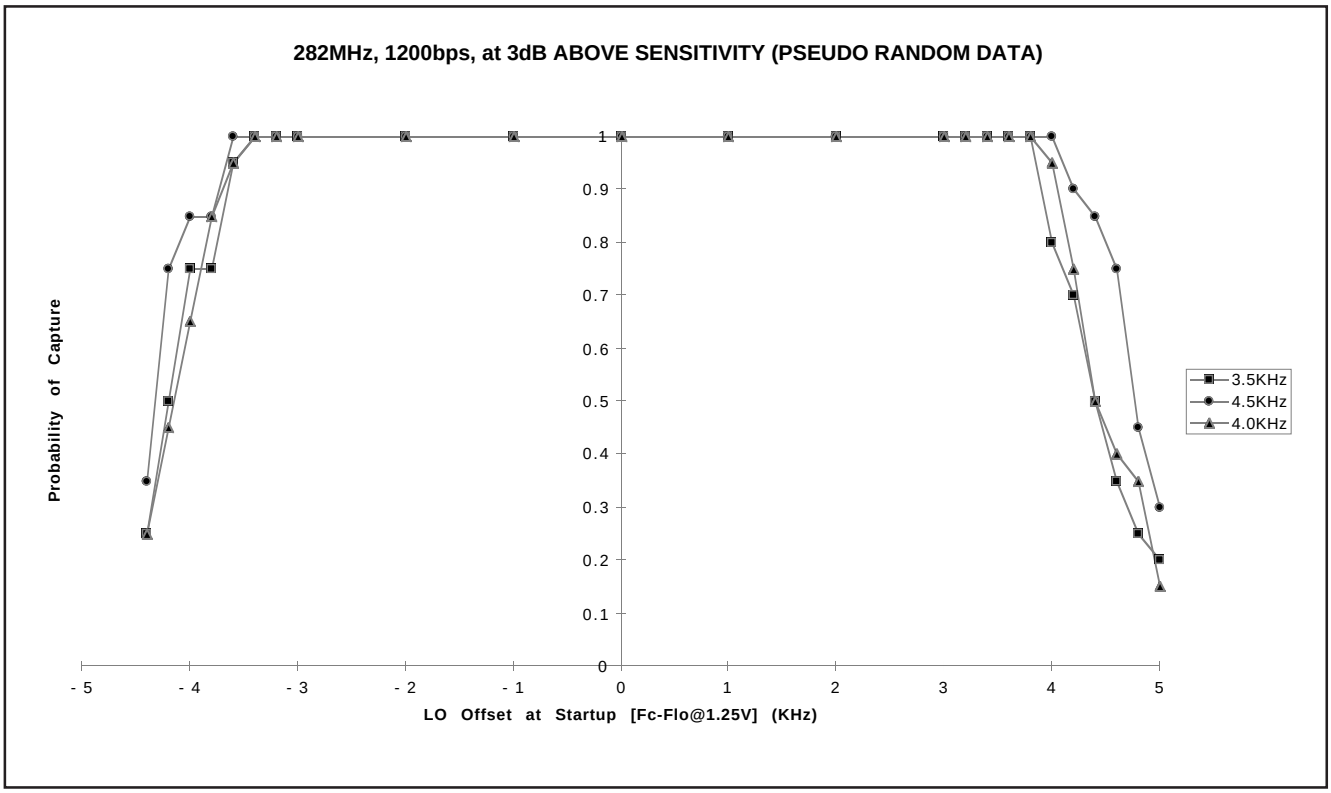


Fig.15 Probability of Capture vs Peak Deviation with BEC (40ms ON / 136ms OFF)

AFC BUFFER

The AFC_OP can supply only a very small amount of current (see Data Sheet). Any DC loading of the AFC_OP pin will distort the AFC's open loop characteristic causing a degradation in capture range and an offset in the frequency that the AFC locks to. It can, however, drive a varactor direct. An op-amp X 1 voltage buffer is provided on the Evaluation Board, which can be connected to the DCFM input of most signal generators to close the AFC loop. Also the AFC_OP control voltage can be monitored at the output of the buffer.

LO / VCXO

The Local Oscillator is a basic Colpitts type configuration. The crystal used is a fifth overtone and its third harmonic is extracted by the output filter(VC2 and L5) before going into the LO phasing network. The regulated voltage from Vreg supplies the oscillator. VC3 controls the amount of feedback to sustain oscillation. When the AFC loop is closed, the control voltage from AFC_OP can be fed directly to the varactor D2 through R18. The overall tuning bandwidth of the VCOX depends largely on the available capacitance swing of the varactor. When an on-board local oscillator is used R4 and R7 in the LO phasing network can be increased to 1Kohm (i.e. 50ohm termination not required) in order to maximise the voltage swing from the oscillator.

BR_CNT

The logic level on Pin 26 controls the cut off frequency of the 1st order bit rate for a given bit rate filter capacitor at Pin 27. The board has been set up for 1200bps i.e. bit rate filter capacitor value at Pin27 is 560pF and a logic zero (0V to 0.1V) at Pin 26. For 512bps and 2400bps the logic at Pin 26 should be open circuit and one respectively. Sensitivity at these baud rates can then be measured in the usual way.

SET-UP PROCEDURES

Fig.16 shows a basic test equipment set-up. Fig.17 and 18 show sensitivity, IP3 and ACR vs test point level. Trade-offs can be made depending which parameter is more important within the overall system.

Measurement Conditions

Fc	=	as labelled on each board
Deviation Freq.	=	4KHz
Baud Rate	=	1200bps
LO Drive	=	-15dBm
Vcc1	=	1.4 V
Vcc2	=	2.7 V
Temp	=	Room Temp

For Evaluation Boards populated to Option 1 level , the following measurements can be made:-

RF input to TP1 gain
RF input to TPLIMI (after gyrator) gain
Terminal sensitivity, IP3, ACR etc.
LO input vs terminal sensitivity, IP3, ACR etc
Audio AGC characteristic
Baud rate control
Battery economising
Closed loop AFC

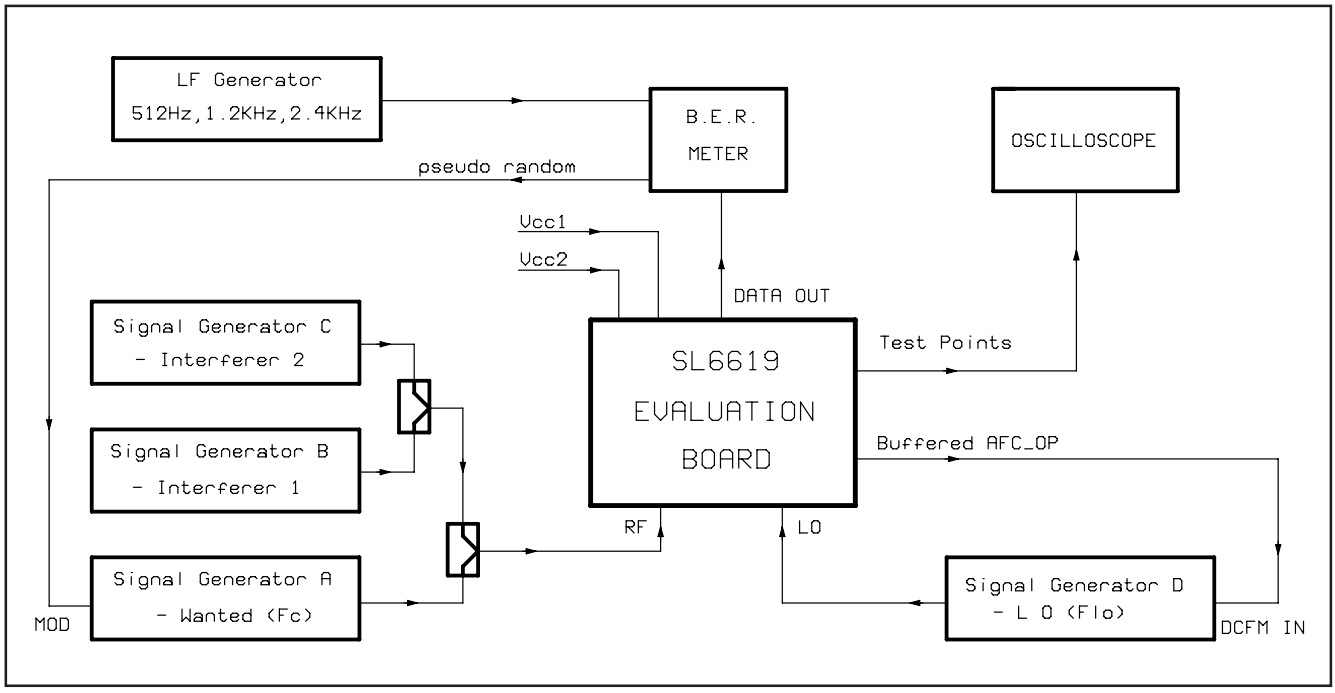


Fig.16

RF input to TP1 & TPQ gain

a. Disconnect link LK2 (disable AGC)
b. Turn OFF signal generators C and B
c. Turn OFF DCFM on signal generator D
d. Using generator D, provide a LO level of -15dBm at the EXT LO port of the board
e. Set frequency of generator D to Fc as labelled on the board
f. Set frequency of generator A to 4KHz above that of generator D
g. Using generator A, provide a RF level of -73dBm at the RF IN port of the board
h. Measure the pk-pk voltages at Pin 8(TPI) and Pin 17(TPQ). They should be 300mV + - 10% pk-pk and in good quadrature.

RF input to TP_LIMI(after gyrator) gain

a. Repeat 1a to 1f
b. Using generator A, provide a RF level of -100dBm at the RF IN port of the board
c. Measure the pk-pk voltage at Pin 29(TP_LIMI) and the level should be 100mV + - 10% pk-pk.
d. To estimate the gyrator filter bandwidth, set the frequency of generator A to 8KHz above that of generator D
e. Re-measure the pk-pk voltage at Pin 29(TP_LIMI) and the level should be 35% of that measured at c.

Terminal sensitivity, IP3, ACR etc.

a. Disconnect link LK2 (disable AGC)
b. Carry out measurements as required base on Mitel Application Note AN197 - 'Performance Measurements on the SL6609A/SL6610 Demonstration Boards' which is included in Appendix A.

LO input vs terminal sensitivity, IP3, ACR etc

a. Disconnect link LK2 (disable AGC)
b. Change LO level (generator D) as desired
c. Carry out measurements as required base on Mitel Application Note AN197 - 'Performance Measurements on the SL6609A/SL6610 Demonstration Boards'.

Audio AGC characteristic

a. Repeat 1a to 1g. Note the pk-pk level of TPI, call it V1.
b. Reconnect link LK2 (enable AGC).
c. Increase the RF level to the RF IN port of the board until the pk-pk level at TPI equals to V1 again and the RF level. This level should be between 20 to 25dB higher than -73dBm.
d. With this set-up configuration, the effect of audio AGC on high level IP3 can be measured as described in Appendix A.

Baud rate control

a. Disconnect link LK2 (disable AGC)
b. Disconnect link LK4 to use external baud rate control
c. Leave BRF_CNT pin OPEN circuit
d. Evaluate the board at 512bps as per Appendix A
e. Connect BRF_CNT pin to 0V
f. Evaluate the board at 1200bps as per Appendix A
g. Connect BRF_CNT pin to Vcc2
h. Evaluate the board at 2400bps as per Appendix A

Battery economising

a. Disconnect link LK2(disable AGC)
b. Connect link LK4 to 0V (for 1200bps)
c. Disconnect link LK3 i.e. use external control
d. Use a function generator to provide 0V to Vcc2 pulses to BEC pin.
e. Start up time may be measured with the help of a storage oscilloscope to monitor time take between the start of an ON pulse and the arrival of good data.

Closed loop AFC - External LO

a. Disconnect link LK2 (disable AGC)
b. Connect link LK4 to 0V (for 1200bps)
c. Connect link LK3 to Vcc2 (constantly ON)
d. Provide +5V and -5V to bias the AFC Buffer
e. Provide, say, -120dBm RF level at the RF IN port with pseudo random modulation and centre frequency of Fc.
f. Connect the buffered AFC_OP to the DCFM input of generator D, set the FM gain to 4KHz/V and enable the DCFM.
g. Monitor the buffered AFC_OP voltage while adjusting the LO frequency until the voltage reaches 1.25V. The frequency of the LO and RF should now be the same.
h. Increase the RF frequency (Fc) by 1KHz the voltage at the buffered AFC_OP should go up by about 300mV and the LO frequency should have followed Fc i.e.1KHz higher. Now the AFC loop is closed and Flo is tracking Fc.
i. All AC measurements can now be performed while the AFC loop is closed.
j. The AFC loop should remain locked for Fc = Flo + - 4KHz

Closed loop AFC - Internal VCXO

a. Disconnect link LK2 (disable AGC)
b. Connect link LK4 to 0V (for 1200bps)
c. Connect link LK3 to Vcc2 (constantly ON)
d. Provide +5V and -5V to bias the AFC Buffer (for AFC_OP monitoring ONLY)
e. Disconnect LK5, reconnect R17 (1K) and C10 (4.7pF)
f. Replace R4 with 1Kohm
g. Set the carrier frequency Fc to that shown in the Mitel Evaluation Results Sheet with pseudo random data
h. Monitor the buffered AFCOP voltage and it should be about +1.25V
i. The AFC loop is now closed and all AC measurements can be carried out as per previous sections

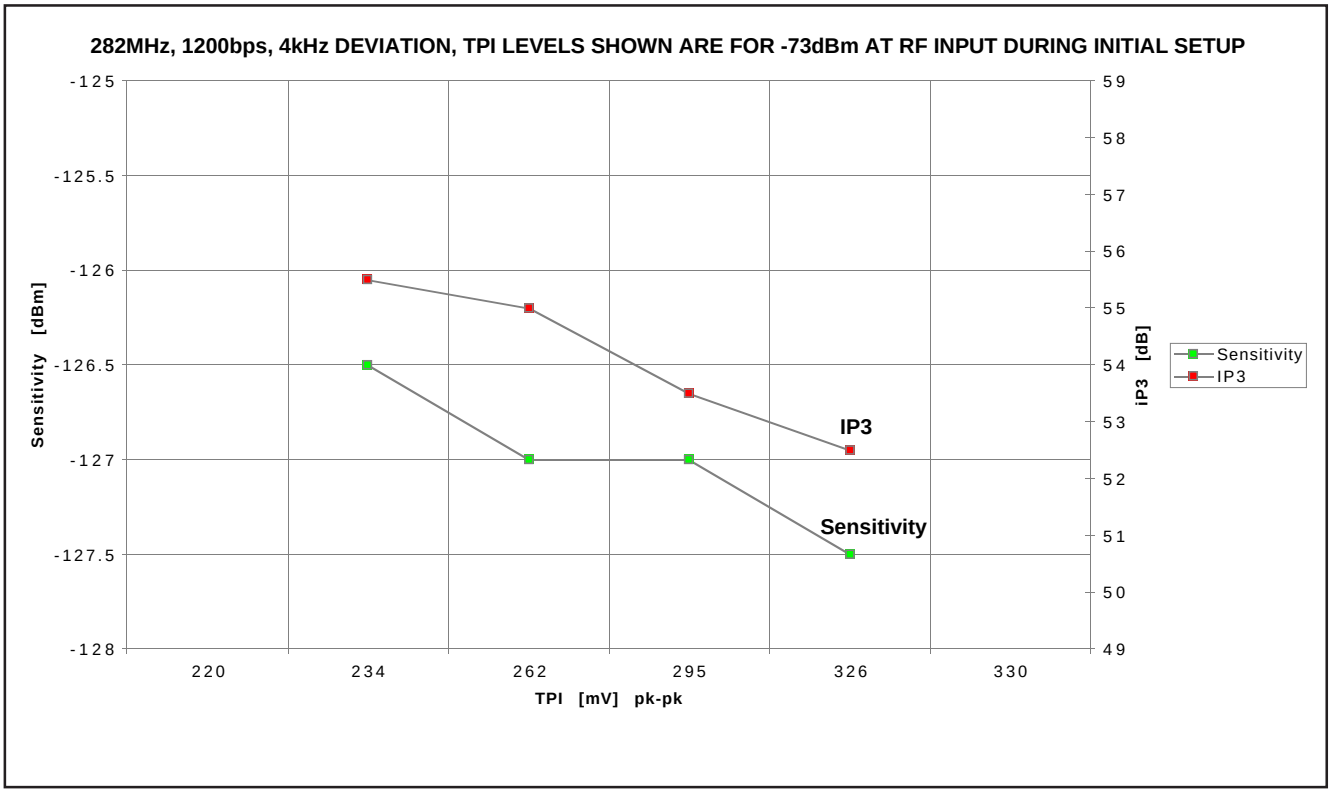


Fig.17 IP3 vs Sensitivity trade-off

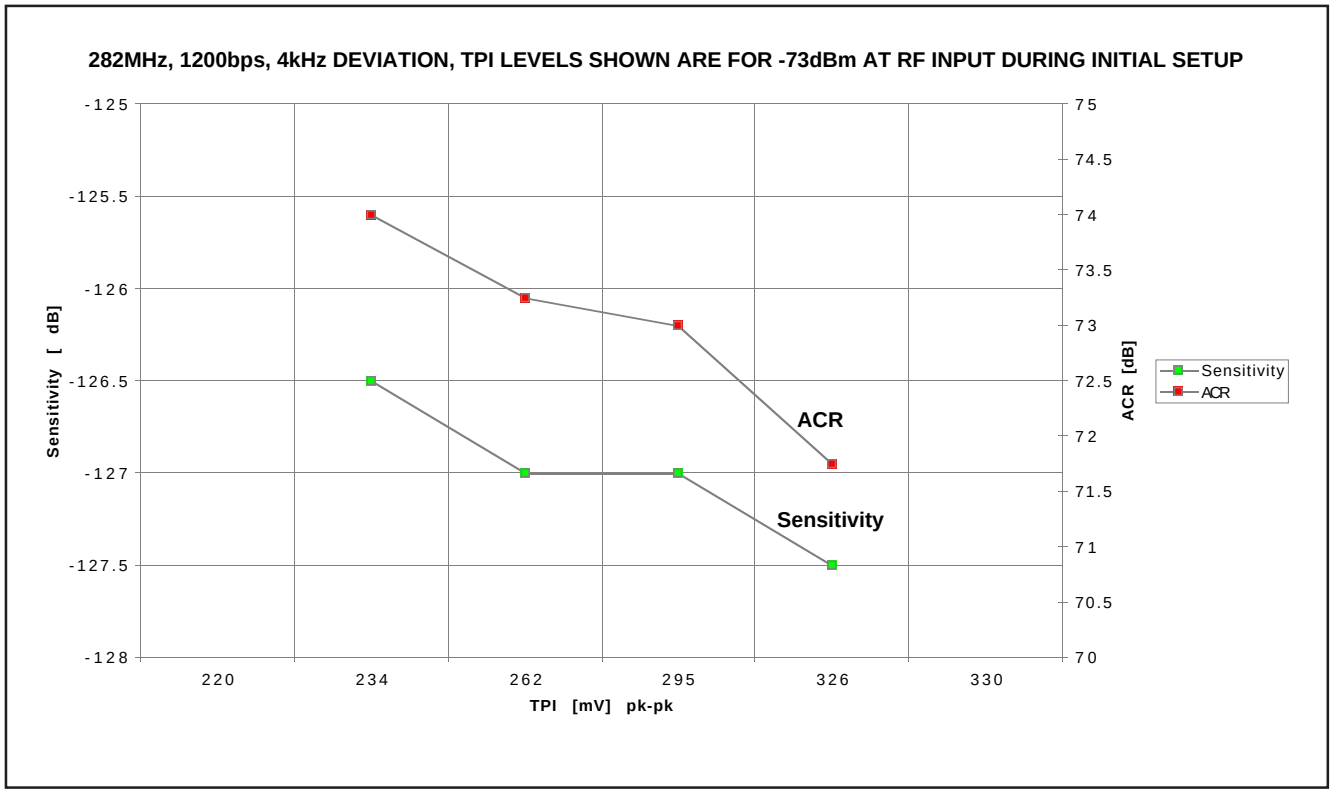


Fig.18 ACR vs Sensitivity trade-off

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